ELECTRONIC INFORMATION DISCLOSURE STATEMENT

Electronic Version v18
Stylesheet Version v18.0

Title of Invention	Method and arrangement for layout and manufacture of nonmanhattan semiconductor integrated circuit using simulated euclidean wiring

Application Number: 09/972011 *09/972011*
Confirmation Number: 5250
First Named Applicant: Steven Teig
Attorney Docket Number: SPLX.P0068
Art Unit: 2825
Examiner: Helen B. Rossoshek
Search string: (4855253 or 5541005 or 5635736 or 5637920 or 5640327 or 5646830 or 5650653 or 5689433 or 5723908 or 5784289 or 5801385 or 5811863 or 5822214 or 5880969 or 5889329 or 5980093 or 6150193 or 6260183 or 6262487 or 6263475 or 6301686 or 6307256 or 6316838 or 6324674 or 6412097 or 6448591 or 6516455 or 20010009031 or 20030025205).pn.

US Patent Documents

Note: Applicant is not required to submit a paper copy of cited US Patent Documents

init	Cite.No.	Patent No.	Date	Patentee	Kind	Class	Subclass
HR	1	4855253	1989-08-08	Weber			
HR	2	5541005	1996-07-30	Bezama et al.			
HR	3	5635736	1997-06-03	Funaki et al.			
HR	4	5637920	1997-06-10	Loo			
HR	5	5640327	1997-06-17	Ting			
HR	6	5646830	1997-07-08	Nagano			
HR	7	5650653	1997-07-22	Rostoker et al.			

09-972011

HR	8	5689433	1997-11-18	Edwards	
HR	9	5723908	1998-03-03	Fuchida et al.	
HR	10	5784289	1998-07-21	Wang	
HR	11	5801385	1998-09-01	Endo et al.	
HR	12	5811863	1998-09-22	Rostoker et al.	
HR	13	5822214	1998-10-13	Rostoker et al.	
HR	14	5880969	1999-03-09	Hama et al.	
HR	15	5889329	1999-03-30	Rostoker et al.	
HR	16	5980093	1999-11-09	Jones et al.	
HR	17	6150193	2000-11-21	Glenn	
HR	18	6260183	2001-07-10	Raspopovic et al.	B1
HR	19	6262487	2001-07-17	Igarashi et al.	B1
HR	20	6263475	2001-07-17	Toyonaga et al.	B1
HR	21	6301686	2001-10-09	Kikuchi et al.	B1
HR	22	6307256	2001-10-23	Chiang et al.	B1
HR	23	6316838	2001-11-13	Ozawa et al.	B1
HR	24	6324674	2001-11-27	Andreev et al.	B2
HR	25	6412097	2002-06-25	Kikuchi et al.	B1
HR	26	6448591	2002-09-10	Juengling	B1
HR	27	6516455	2003-02-04	Teig et al.	B1

US Published Applications

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init	Cite.No.	Pub. No.	Date	Applicant	Kind	Class	Subclass
HR	1	20010009031	2001-07-19	Nitta et al.	A1		
HR	2	20030025205	2003-02-06	Shively	A1		

Signature

Examiner Name	Date
Helen Rossoshek	11/08/2004

Based on PTO/SB/08 a & b (05-03)
Approved for use through 05/31/2003. OMB 0651-0031
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Sheet 1 of 1

Application Number	09/972,011
Filing Date	10/5/2001
First Named Inventor	Steven Teig, et al.
Group Art Unit	2825
Examiner Name	Helen Rossoshek
Attorney Docket Number	SPLX.P0068

FOREIGN PATENT DOCUMENTS

Examiner* Initials	Cite No.[1]	Foreign Patent Document: Office[3]	Number[4]	Kind Code (if known)[5]	Date of Publication MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]
HR	1.	JP	04-000677		01-06-1992	Fujiwara et al.	with English translation of Abstract;	
HR	2.	JP	2000-082743		03-21-2000	Igarashi et al.	with Japanese Patent Office's English translation of Abstract; and with English translation of the application.	√

NON PATENT LITERATURE DOCUMENTS

Examiner* Initials	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[6]
HR	3.	Chen et al., Optimal Algorithms for Bubble Sort Based Non-Manhattan Channel Routing, May 1994, Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions Volume: 13 Issues, pp. 603-609.	
HR	4.	Chen, H. et al., Physical Planning of On-Chip Interconnect Architectures, 2002, IEEE, International Conference, pp. 30-35	
HR	5.	Cong J. et al., DUNE – A Multilayer Gridless Routing System, May 2001, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol 20, iss. 5, pp. 633-647.	
HR	6.	Dion J. et al., Contour: A Tile-based Gridless Router, March 1995, Digital Western Research Laboratory, research Report 95/3, pp.1-22	
HR	7.	Merriam-Webster's Collegiate Dictionary, 10th edition, Merriam-Webster Incorporated, p.606	
HR	8.	Schiele, W. et al., A Gridless Router for Industrial Design Rule, 27th ACM-IEEE Design Automation Conference, pp. 626-631, 1990.	
HR	9.	Tseng H. et al., A Gridless Multilayer Router for Standard Cell Circuits Using CTM Cells, Oct. 1999, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol 18, iss. 10, pp. 1462-1479.	

Examiner Signature	Helen Rossoshek	Date Considered	11/08/2004

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HR	2	20030025205	2003-02-06	Shively	A1		

Signature

Examiner Name	Date
Helen Rohoshelo	11/08/2004